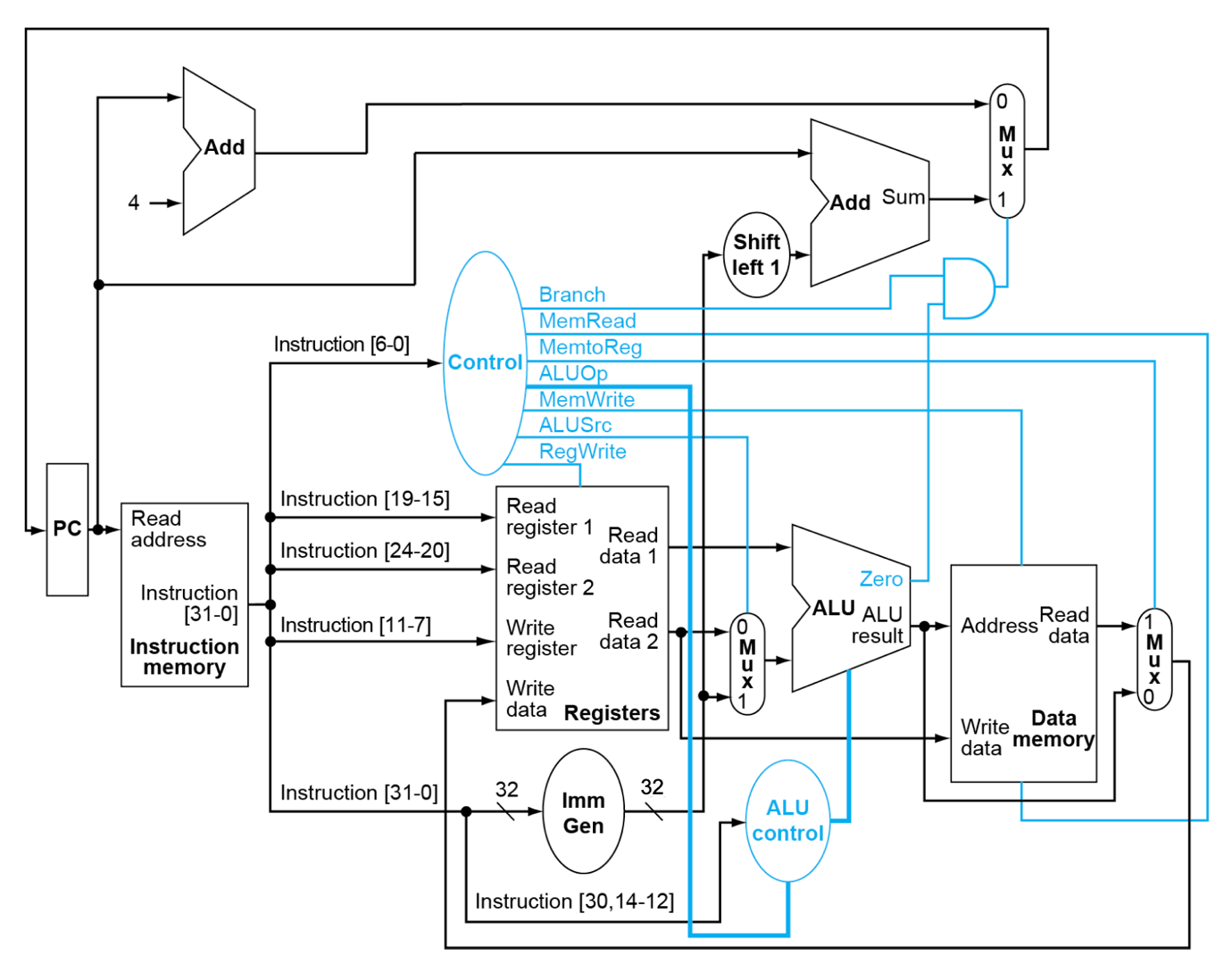
VE370 Lab 2 Report

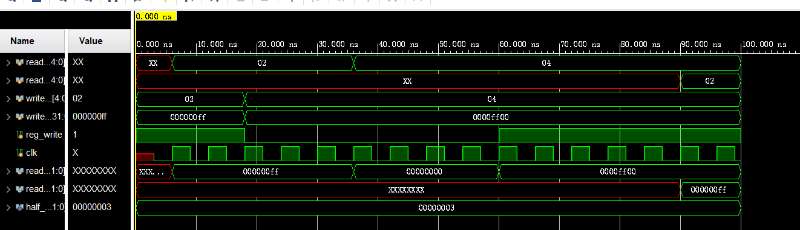
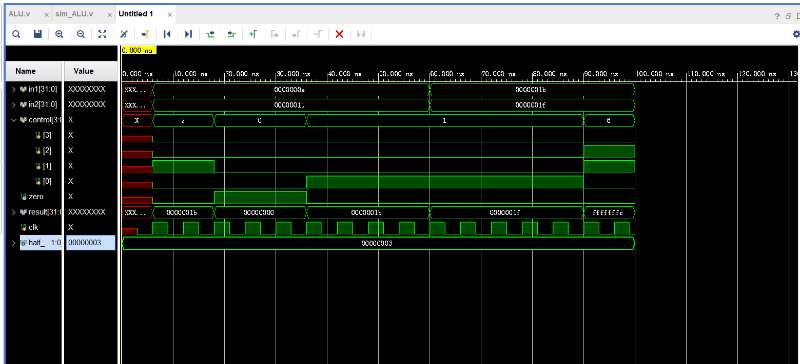
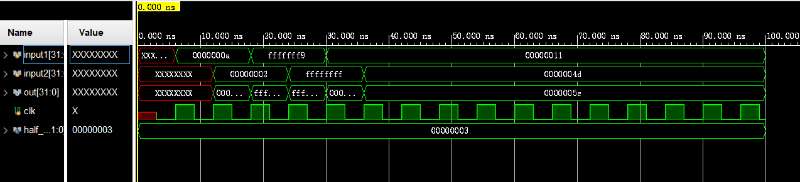
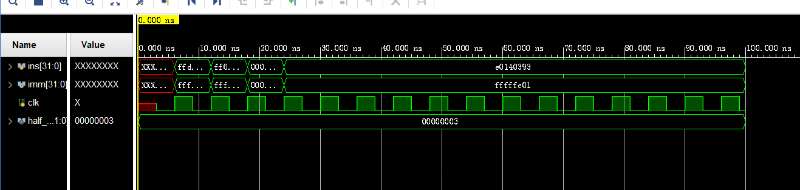
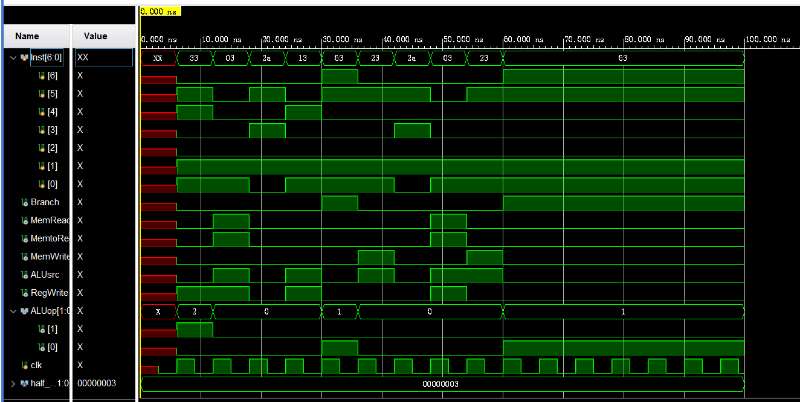
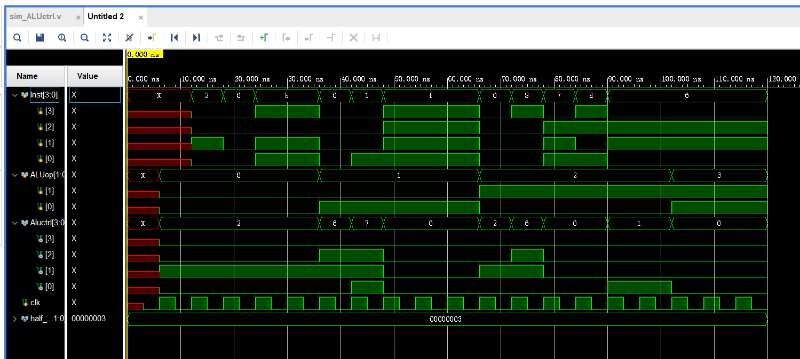
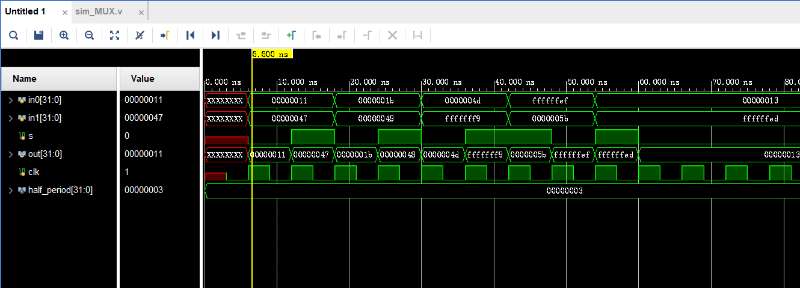
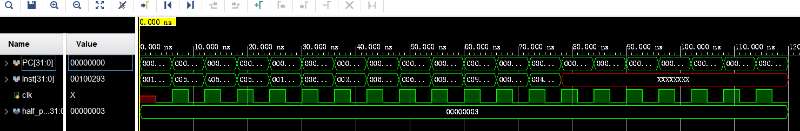
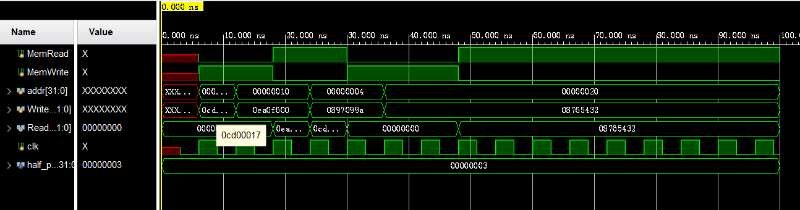
Kaiqi Zhu 522370910091

1. Brief Description

This is the structural design of the single cycle processor. All the shapes such as circles and rectangles are modules in Verilog, and the lines are wires or registers stored in the programs.

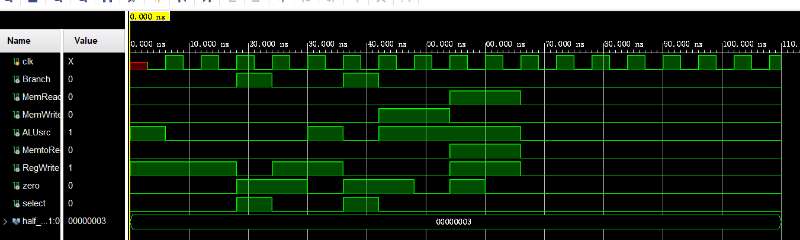
1. Simulation Results for Modules

The graphs of simulation result for each module are shown below:

1. Register File
2. ALU
3. Adder
4. Immediate Generator
5. Control Unit
6. ALU Control
7. MUX
8. Instruction Memory
9. Data Memory

All of the simulation results demonstrated in the graph can show that each module used in the top module can function properly.

1. Simulation Results for Instructions

The simulation result graph is shown below:

In addition, a set of instructions is given to verify the needed operations. In the instructions, all types of the needed instructions are tested. The RISC-V codes are:

addi t0 x0 -10

add t1 t0 t0

sub t2 t0 t1

and t3 t1 x0

or t4 t1 t0

sw t4 0(x0)

sw t0 4(x0)

beq t0 x0 L1

add t4 t1 x0 # possible error

L1: bne t1 t4 error1

bne t1 t3 L2

error1: add t2 x0 x0

L2: lw s0 0(x0)

lw s1 4(x0)

addi s1 s1 8

beq s0 s1 L3

error2: add t2 x0 x0

L3: add t2 t2 t2

and the corresponding machine codes are:

regs[0] = 32'hff60\_0293;

regs[1] = 32'h0052\_8333;

regs[2] = 32'h4062\_83b3;

regs[3] = 32'h0003\_7e33;

regs[4] = 32'h0053\_6eb3;

regs[5] = 32'h01d0\_2023;

regs[6] = 32'h0050\_2223;

regs[7] = 32'h0002\_8463;

regs[8] = 32'h0003\_0eb3;

regs[9] = 32'h01d3\_1463;

regs[10] = 32'h01c3\_1463;

regs[11] = 32'h0000\_03b3;

regs[12] = 32'h0000\_2403;

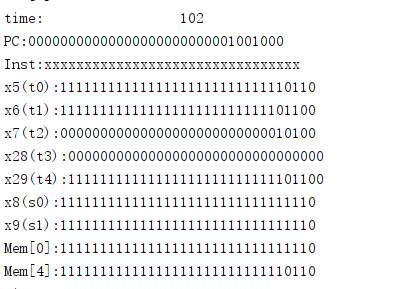
regs[13] = 32'h0040\_2483;

regs[14] = 32'h0084\_8493;

regs[15] = 32'h0094\_0463;

regs[16] = 32'h0000\_03b3;

regs[17] = 32'h0073\_83b3;

Based on the instructions, the outputs shown in the log window are

which is in accordance with the expected result. Therefore, the simulation results can show that the program can function properly.

1. RTL schematic

The detailed RTL schematic based on the codes generated by Vivado is shown below:

References:

1. VE370 Lab 2 Manual FA24
2. VE370 T5 Slides FA24, Gang Zheng